ENGSYS 632
Ecole Doctorale

Graduate School ENGineering and SYstems Sciences

Sujet thèse / PhD subject 2024

Titre Thèse	Sustainable and strategic technology 2D-InSe-based-Field Effect Transistors for high frequency applications	
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Projet phare (principal)	Micro-Nano-devices et Telecom UHD	
Demande thèse labelisée IEMN	Non	
Financement demandé	Contrat Doctoral Etablissement	ULille ☐ Centrale Lille ☐ JUNIA ☐
	Région –X Préciser :	Co financement (Préciser l'origine, demande en cours, acquis ou pas) : ANR AAP2024 en cours
Financement acquis ☐ **Financement partiellement acquis** ☐	Contrats de Recherche ☐ Préciser :	Autre ☐ Préciser :

Résumé du sujet :

- **Context: issue of III-V technologies for future societal needs**

III-V technologies on InP substrate, making use of Indium and Gallium alloys, have shown their capabilities for high performance electronic and photonic applications, by demonstration of their superiority for high-speed communication and sensing. These excellent performances are related to the high mobility of III-V materials, possibilities of energy band engineering and direct bandgap. This technology is considered for the next mobile network 6G where a high bit data rate of 100Gbit/s is targeted and is also at the heart of many THz devices [1] [2]. This data rate increase is mandatory to meet the growing demand from remote work, online education, shopping, entertainment, and recently by Internet of Things (IoT) needs. Indeed, the IOT will require the deployment of connected objects, whose number is expected to increase from 30 billions in 2020 to 100 billions in 2050 [3].

However, III-V technologies suffer from their cost and the scarcity/accessibility of the materials used. Indeed III-V materials are grown on InP or GaAs substrates, which suffer from their low substrate diameter and high cost. Moreover, the scarcity of Gallium and Indium will have a major impact on development of III-V based mass application. Indeed, the Indium and Gallium reserves are limited on Earth. Moreover, the main country of production is China (75% and 96.3% for Indium and Gallium respectively). Finally, Gallium and Indium production have significant environmental consequences, like all mining and refinery production. The extraction and purification processes of these elements are complex techniques, expensive in energy and water.

- **Motivation of the work**

To reduce the geopolitical dependence to these raw materials and defend France and European Sovereignty, conserve the natural reserves and preserve the environment, the use of Gallium and Indium should be limited. For high frequency microelectronics applications, one solution is to avoid the use of Ga or In-based substrates and to use two-dimensional materials (2DMs) as the active material of the transistor since only a few layers of 2DMs are required to form the transistor channel. **In this thesis, we propose to develop technology for fabrication InSe-based Field Effect transistors (FET) on silicon substrate**. The particular structure of 2DM leads to the absence of surface dangling bonds and favours free integration [4] within heterostructures based on the numerous possibilities offered by material combinations without any lattice matching requirement. Then, 2DM offers the possibility to be integrated on Silicon wafer, which is today the useful substrate for mass production and does not content any rare material.

Scaling down rules of FET requires thinning the channel by the same factor as the gate length to guarantee sufficient electrostatic control and to suppress short channel effect (SCE). The SCE is an important source of limitation in digital applications as it degrades the subthreshold behaviour. In analogue application, the SCE affects the cut-off frequency of the FET, which is fundamental for high gain, low noise and power capabilities at high frequency. To keep the aspect ratio constant in the scaling down rule, it is then necessary to reduce the channel thickness to the required values. However, the charge scattering at the interfaces in standard bulk material, results in a drastic degradation of the carrier mobility in the channel, which ruins device performance. The use of 2DMs as channel material might be a solution, because they are self-passivated and hence, the charge carrier mobility is not strongly affected by surface scattering.

InSe is a 2DM, with an indirect band gap of 2.2eV at monolayer thickness, which becomes direct above a few monolayers before reaching a bulk value of 1.26eV [5]. This direct band gap offers possibilities for photonic applications in the range from visible to infrared, with a better photo response than Graphene or MoS_2 [5]. InSe may also show promise for memristor manufacturing [6], thermoelectricity [7]. For electronic applications, a carrier mobilities are found to exceed 10^3 cm^2/Vs and 10^4 cm^2/Vs at room and liquid-helium temperatures [82] and an I_{ON}/I_{OFF} ratio of 10^8 was achieved on a FET [93], making it an interesting candidate for transistor manufacturing.

- **Actions of the thesis**

The objective of the thesis is then to develop technological process and explore the potential of InSe for FET on Silicon substrate. This work is very closely linked to the MBE growth activity of the EPIPHY group of the IEMN. EPIPHY group will supply the InSe material growth on Silicon substrate. However, a microelectronic grade 2D-InSe material may not be available at the start of the thesis. Thus, exfoliation will be also explored at the beginning to start the development of the main technological steps: ohmic contact and Metal Oxide Semiconductor contact (MOS). We will conduct a study to obtain Ohmic contacts by varying the choice of metal, surface preparation, annealing temperature and time. The second step will aim at the realization of the gate contact whose main element is the oxide. Two solutions will be considered: native oxide or the growth of an oxide by ALD. Particular attention will be paid to the quality of the semiconductor oxide interface. These contacts will be explored by specific tools: atomic force microscopy (AFM), scanning electron microscopy (SEM), X-ray diffraction and Raman spectroscopy. Finally, the transistors will be completely fabricated on InSe-Silicon substrate followed by a deep characterization in DC and on-wafer microwave (up to 110GHz).

At the end of the thesis, the student will have acquired skills in cleanroom technology, physico-chemical and electrical characterizations (DC and RF), which is an asset today for its future professional integration.

[1] H. Gao, 2023 IEEE MTT-S International Wireless Symposium (IWS), 2023.
[2] M. Kim et al., Nature Electronics, vol. 5, p. 367–373, 2022.
[3] M. Capra et al., Future Internet, vol. 11, p. 100, 2019.
[4] M. Zeng. et al, Chemical reviews, vol. 13, pp. 6236-6296, 2018.
[5] Z. Yang et al., ACS Nano, vol. 11, pp. 4225-4236, 2017.
[6] Q. Li et al, Int. J. extrem. Manuf., vol. 3, p. 045103 , 2021.
[7] H. Shi et al., Aggregate, vol. 2, 2021.
[8] D. A. Bandurin et al., Nature Technology, vol. 12, p. 223, 2017.
[9] J. Jiang et al., Nature, vol. 616, pp. 470-475, 2023.