

## **Benefits of a nano-patterned thin silicon film based thermoelectric generator**

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Developing silicon based thermoelectric generators is subject to high interest in the thermoelectric energy harvesting community. Compared to current materials used for commercial thermoelectric generators, silicon has the advantages to be the most wide spread semi-conductor material, environmentally less harmful and to already have facilities and processing technologies developed for low cost mass production. However, the high thermal conductivity of bulk silicon makes it a very bad thermoelectric material especially for near room temperatures applications. Hence, thermal conductivity reduction is the key to upgrade silicon as an efficient thermoelectric material. Efforts for thermal conductivity reduction are oriented toward reducing the phonon contributions, which are the dominant contribution. This reduction can be achieved by reducing the phonon mean free path and/or the phonon group velocity e.g. use of thin films [1], nanowires [2], add of impurities [3], Silicon nano-patterning [4]. Besides, in this paper we focus on Silicon thermoelectric properties improvement and on the development of a planar thin silicon film based thermoelectric generator. The expected performances are benchmarked regarding existing commercial thermoelectric generator. In our work, periodical holes called phononic crystal are patterned on the silicon thin film to downscale further the thermal conductivity with minor impact on the electrical conductivity. The combination of the thin film and the phononic crystal allows us to reach a thermal conductivity of  $34 \text{ W} \cdot \text{m}^{-1} \cdot \text{K}^{-1}$  [5] and can even allow us to reach  $2 \text{ W} \cdot \text{m}^{-1} \cdot \text{K}^{-1}$  [4]. We performed a FEM benchmarking of our optimized thin silicon based TEG with the commercial Micropelt<sup>®</sup> TEG [6], [7] for  $20 \text{ W} \cdot \text{m}^{-1} \cdot \text{K}^{-1}$  and  $4 \text{ W} \cdot \text{m}^{-1} \cdot \text{K}^{-1}$  as silicon's thermal conductivity, near room temperatures range and for two configurations of cooling conditions : natural convection without heat sink and natural convection with a small heat sink. Results show an improved exploitation of the thermal gradient into the thermoelectric material due the planar architecture thus leading to a maximized harvested energy even without a massive heat sink. Those results open perspectives in the field of autonomous sensor nodes based on low cost and scaled silicon material production.

### **Bibliography:**

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